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M60066PCT

WHAT IS CLAIMED IS:

1. A method of manufacturing a heterobipolar transistor, wherein epitaxially grown layers (12) on a substrate (1) are structured by etching, characterized in that an emitter contact (31) and a base contact (32) are formed by simultaneous metallizing of an emitter layer (11) and a base layer (6).
2. The method as claimed in claim 1, characterized in that when metallizing, platinum is vaporized.
3. The method as claimed in claim 1, characterized in that successive metal layers of platinum, titanium, platinum and gold are vapor deposited when metallizing.
4. The method as claimed in claim 1, characterized in that, prior to metallizing the emitter layer (11) and the base layer (6), an emitter structure (21) is etched in consideration of crystal orientation and material selection so that etching edges (22, 23) of the emitter structure (21) will have an undercut, the etching of the emitter structure (21) being stopped in the zone of a spacer layer (7) or the base layer (6).
5. The method as claimed in claim 4, characterized in that, prior to etching the base layer (6), a photoresist layer is applied around the etched emitter structure (21) so as to fully surround the emitter structure (21) with photoresist material (40) and in such a way that at least part of a surrounding portion (41) of the base contact (32) remote from the emitter structure (21) will not be covered by photoresist material (40).
6. The method as claimed in claim 1, characterized in that a metallic base lead (91) extending between the base contact (32, 90) and a base connection port (92) is completely etched under, whereby an air bridge results.

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7. The method as claimed in claim 1, characterized in that a collector structure (53) is formed upon structuring of the base layer (6) and between two successive lithographic steps.
8. The method as claimed in claim 7, characterized in that at least part of the collector structure (53) is etched in consideration of material selection so that etching edges (51, 52) of the collector structure (53) will have an undercut, the etching being stopped on a subcollector material (2).
9. The method as claimed in claim 1, characterized in that the epitaxially grown layers are formed at least partly of III-V semiconductor materials.